# Fast and Accurate Ramp Generation with a PLL-Stabilized 24-GHz SiGe VCO for FMCW and FSCW Applications

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*Abstract* — **In Microwave sensor systems the application of linear frequency modulation schemes as well as frequency stepping is commonly used. In this paper we describe the generation of fast and highly accurate frequency ramps by means of a fractional-N-PLL stabilized integrated 24-GHz voltage controlled SiGe oscillator, which are a prerequisite for high achievable measurement accuracies. Linearity measurements with phase evaluation on fabricated devices have shown an RF-phase deviation of less than 1.5 rad for a linear frequency sweep with a bandwidth of 250 MHz at 24.5 GHz and a sweep duration of 250 µs.**

## I. Introduction

The oscillator is a crucial component in every microwave system. Historically Gunn-Oscillators have been in widespread use. Nowadays, III-V semiconductor devices like PHEMTs are widely used, but suffer under the expensive technology.

A low-cost alternative which promises commercial success is the application of Silicon Germanium (SiGe) devices. Due to advances in process technology and reduced structure size the fabrication of very reasonable microwave semiconductors operating in the 24 GHz ISM-band and above is possible [1, 2].

For integration purposes stabilization by a dielectric resonator is unsuitable. In this contribution we present a fractional-N-PLL stabilization technique for an integrated microwave oscillator which can be used for common radar modulation schemes like linear frequency modulation (LFM) and frequency stepping (FS).

The attainable accuracy of a microwave radar sensor strongly depends on the phase deviation of the linear frequency sweep [3] or the accuracy of the frequency steps. This is valid for a simple fast Fourier transformation (FFT) evaluation and is even more important for the application of highly sophisticated frequency estimation algorithms. The integration of the whole signal generation unit leads to a highly integrated and compact device for sensor signal generation. For near-range radar applications up to some 100 m the error introduced by the achieved sweep nonlinearity would be less than 1 mm and therefore negligible.

## II. 24-GHz SiGe VCO-Chip

The fully integrated VCO with on-chip output buffer and frequency divider is fabricated in a 0.35-µm production SiGe technology (B7HF-process) by Infineon Technologies.

The oscillator is essentially a differential negative resistance LC-oscillator. The operating frequency is determined by a fully integrated tank consisting of varactor, metal-insulator-metal (MIM) capacitors and high-Q spiral inductor.

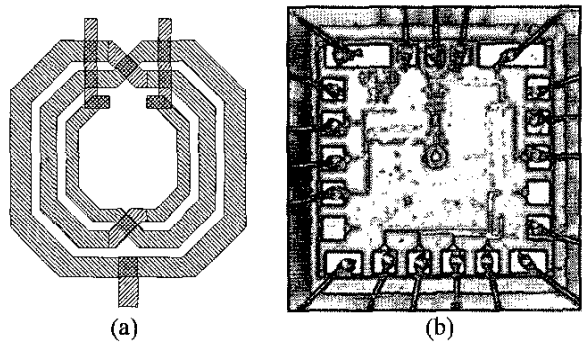


Fig. 1. (a) Layout of the high-Q integrated inductor and (b) chip photograph of the wire-bonded oscillator chip with integrated output buffer and frequency divider.

The inductor is an optimized three-turn spiral inductor with a diameter of 60 µm. A sketch of the layout is depicted in Fig. 1(a), Fig. 1(b) shows a photograph of the wire-bonded 24-GHz VCO chip, including output buffer and frequency divider.

To reduce series resistance, the inductor is realized on the thick top-metal layer with a thickness of 2.8 µm and has a wider trace width in the outer turns. The measured



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quality factor of 13 at 20 GHz for the 390-pH spiral inductor agrees very well with simulation results obtained by using commercial field-solvers.

Due to the high quality factor of all tank components, good phase-noise performance is achieved. The measured phase noise of the integrated VCO is -100.5 dBc/Hz at 1 MHz offset from the carrier. The corrected output power of the chip, taking into account bondwire loss, connector loss, transmission line and cable losses, is about 0 dBm. The measured spectrum of the free-running oscillator is shown in Fig. 2.

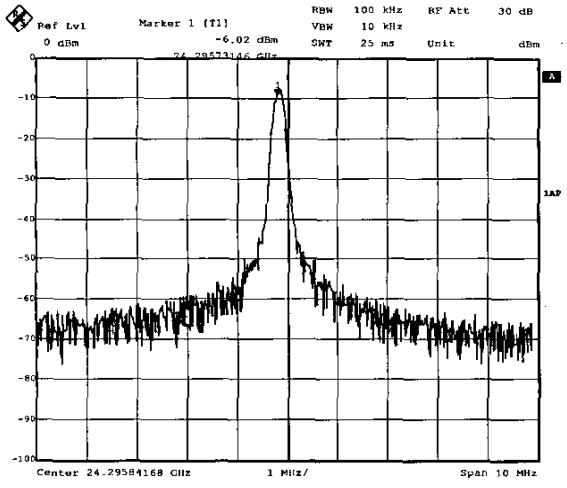


Fig. 2. Measured phase noise of the VCO at 24.3 GHz. This corresponds to -100.5 dBc/Hz @ 1 MHz off carrier.

In addition to the VCO, an output buffer is integrated on the chip. With a given transistor cut-off frequency $f_T$ of 75 GHz, the current gain around 24 GHz is approximately equal to three. Thus the output buffer is realized by several stages of emitter-followers and differential amplifiers with increasing bias currents in every stage. On-wafer measurements exhibited an output power of 0 dBm.

The integrated frequency divider is important for stabilization, to make the oscillator chip compatible with existing PLLs, without an external prescaler. Every dividing stage consists of a master-slave flip-flop with a feedback-loop operating the device as toggle-flip-flop, and halves the frequency. The four stages together divide the 24-GHz signal by 16, resulting in an output frequency of 1.5 GHz. The divider is designed to have its self-resonance frequency in the range of the operating frequency in order to reduce the input power necessary to drive it.

For measurement purposes the VCO-chip is wire-bonded on alumina substrate and equipped with a 3.5-mm connector for the RF output and an SMA-connector for the divided output. Overall current consumption is 80 mA at a supply voltage of 3.6 V. The tuning range can be designed from some hundred MHz to more than 2 GHz [4].

## III. Stabilization and Ramp Generation

For the application of the VCO within allowed ISM-frequency bands a stabilization technique is necessary. Dielectric resonators for example are no viable solution for integration and still need tuning. PLL-techniques as an alternative allow stabilization with high accuracy and fine tuning steps, if fractional-N-PLL-techniques are used. With the proposed additional ramp generator, a linear modulation can be performed with the same circuit.

### *A. Fractional-N-PLL Stabilization*

In Fig. 3 the basic functional blocks of the stabilization and ramp generation unit are shown.

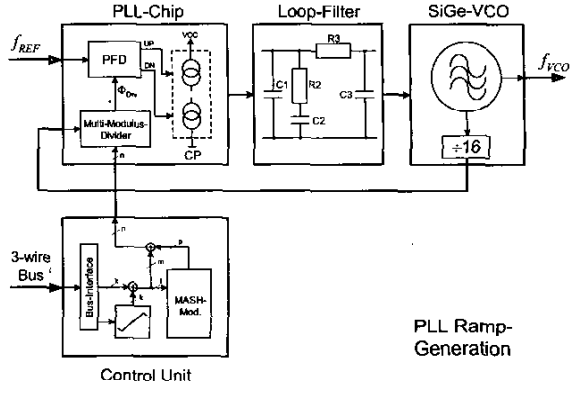


Fig. 3. Basic functional blocks of the ramp generation unit with stabilization and modulation capabilities.

The designed PLL-chip with multi-modulus divider, phase frequency discriminator (PFD), and charge pump (CP) is realized in silicon bipolar technology and can be operated with a reference clock frequency of up to 150 MHz [5].

In this design-stage the control logic is realized in an external FPGA and combines a MASH modulator of 3rd order with a ramp generator programmable via a three-wire bus interface.

Ramp generation is done by changing the input value to the MASH modulator in an appropriate way. Frequency steps for FSCW applications are obtained with a step-rate slow enough for the PLL to settle to the desired frequency value. In contrast, when generating fast linear chirps, the PLL never fully settles but shows an – ideally constant – phase offset to the input value. In this case a high tuning linearity helps to reduce the remaining phase deviation.

Fig. 4 shows the measured spectrum of the stabilized oscillator, locked at 24.5 GHz.

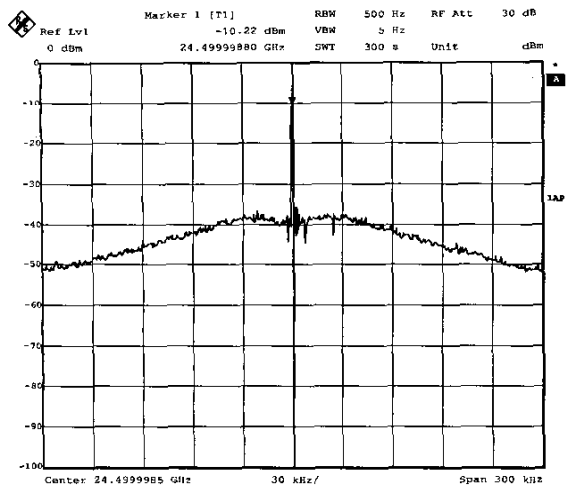


Fig. 4. Measured spectrum of the PLL-stabilized oscillator with a loop-bandwidth of 100 kHz.

## IV. Measurement Setup and Results

The measurement of linear chirps at higher frequencies is difficult and cannot be handled with conventional microwave measurement equipment. One possibility is to mix the ramp with a time shifted version of its own signal produced e.g. by a lengthy cable and consider the obtained spectrum in the IF [6]. This can give an approximation of the overall nonlinearity but no insight into the detailed sweep behavior. A setup with two synchronized and slightly shifted frequency ramps [7] results in a measurement of the superposition of two independent frequency deviation errors. Instead, we use a measurement setup, as shown in Fig. 5 for ramp measurements.

With a highly stable reference oscillator the chirp is downconverted to a frequency range where it can be sampled with high accuracy by a digital storage oscilloscope (DSO). A trigger line ensures a synchronized start of the sweep which is necessary for a stationary picture on the screen but not for data capturing. Applying the discrete Hilbert transformation (DHT) by means of the discrete Fourier transformation (DFT) [8] to the digitized data $y(n)$ we get

$$Y(k)=\sum_{n=0}^{N-1} y(n)e^{-jw}, \quad w=2\pi\frac{nk}{N} \tag{1}$$

$$V(k)=-j\,\mathrm{sgn}(N/2-k)\,\mathrm{sgn}(k)\,Y(k), \tag{2}$$

$$v(n)=\frac{1}{N}\sum_{k=0}^{N-1} V(k)e^{jw}. \tag{3}$$

Next we build the analytic signal $y^+(n)$

$$y^+(n)=y(n)+jv(n) \tag{4}$$

and compare the argument, which is conserved by the downconversion, with the argument of an ideal chirp, described by the slope $K$ of the frequency sweep and starting at $f_0$-$f_{LO}$; $f_S$ denotes the sampling frequency.

$$\delta\varphi(n)=\arg\{y^+(n)\}-\arg\left\{e^{j2\pi\left(\varphi_0+\frac{f_0-f_{LO}}{f_S}n+\frac{K}{2f_S^2}n^2\right)}\right\} \tag{5}$$

This method gives detailed insight into the full course of the sweep, down to the actual signal phase, which is important for an estimation of the error in practical radar applications.

### A. FSCW Ramp Measurements

Frequency steps of the VCO, as shown in Figs. 6 and 7 are evaluated in a similar manner. The long step time of 100 µs is chosen to be able to verify the results with a fast frequency counter. The frequency error is less than $4\cdot10^{-8}$.

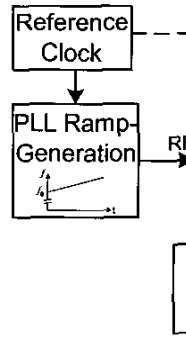


Fig. 5. Measurement setup for the highly accurate measurement of fast ramps at high frequencies.

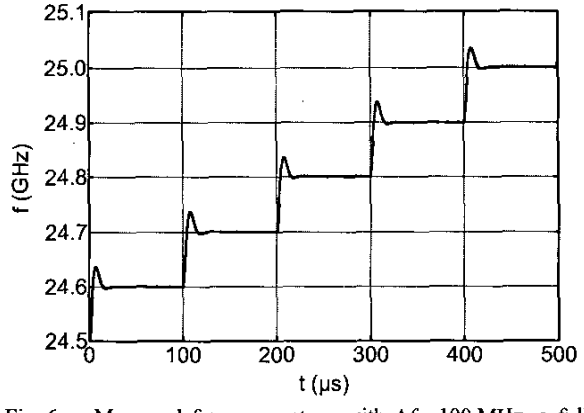


Fig. 6. Measured frequency steps with $\Delta f$ = 100 MHz, a full sweep bandwidth of 500 MHz, and a step time of 100 µs.

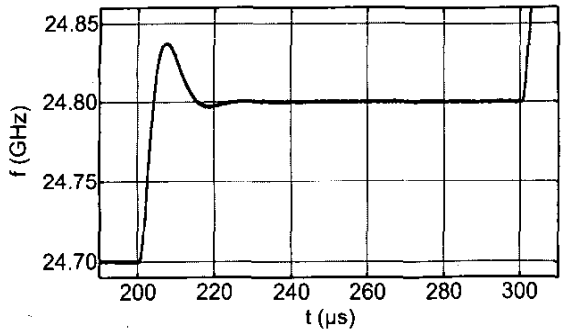


Fig. 7. Detail of the transient response of a 100-MHz frequency step.

*B. LFMCW Ramp Measurements*

In Fig. 8 the measurement of a fast and highly linear frequency ramp is shown. The starting frequency is 24.5 GHz. The LO frequency is chosen to be 5 MHz below, and the sampling rate of the oscilloscope is 1 GHz. In Fig. 9 the deviation from the ideal phase during the whole sweep is plotted.

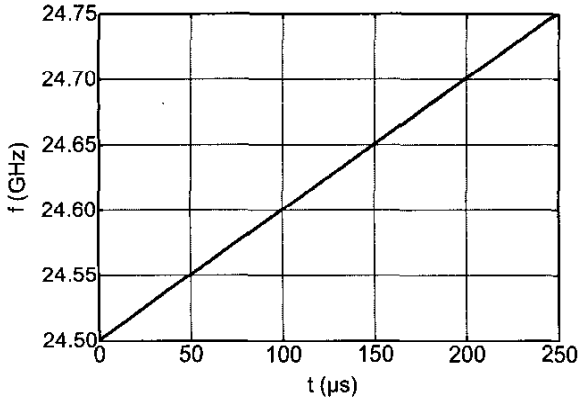


Fig. 8. Highly linear frequency ramp with 250 MHz bandwidth and a sweep rate of 1 MHz/μs starting at 24.5 GHz.

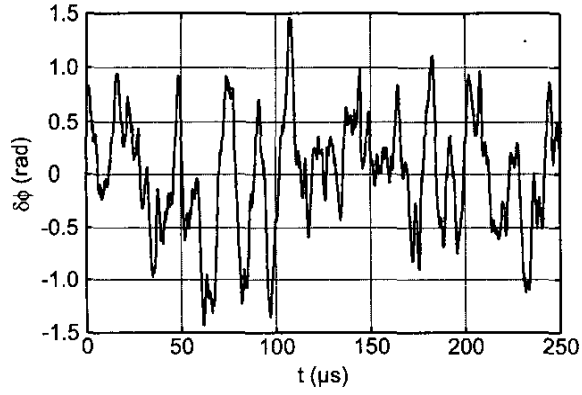


Fig. 9. Measured phase deviations of less than 1.5 rad for a linear frequency sweep of 250 MHz bandwidth within 250 μs.

## V. Conclusion

A ramp generation unit operating directly at 24 GHz was presented. A fractional-N-PLL technique is used for the stabilization and generation of highly linear and fast frequency ramps, which are common in microwave sensor applications. Frequency ramps with sweep rates of 1 MHz/μs and bandwidths greater than 500 MHz showed a phase deviation of less than 1.5 rad. With this linearity the error introduced by frequency deviations of the sweep is negligible in most applications.

## Acknowledgement

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## References

[1] K. Ettinger, A. Stelzer, C. G. Diskus, W. Thomann, J. Fenk, R. Weigel, "Single-Chip 20-GHz VCO and Frequency Divider in SiGe Technology," *IEEE MTT-S International Microwave Symposium*, Seattle, Washington, vol. 2, pp. 835–838, June 2–4, 2002.

[2] G. Ritzberger, J. Bock, and A. L. Scholtz, "45 GHz highly integrated phase-locked loop frequency synthesizer in SiGe bipolar technology," *IEEE MTT-S International Microwave Symposium 2002*, Seattle, WA, USA, pp. 831-834, 2002.

[3] J. Wang Dong, X. Hu, and J. Ruan Wen, "Analysis of the Influence of the FM Non-Linearity on the Range Resolution of LFMCW Radar," *Asia Pacific Microwave Conference 1999*, Singapur, 1999.

[4] K. Ettinger, A Stelzer, J. Höftberger, C. G. Diskus, and R. Weigel, "Single-Chip 19 and 24-GHz VCO and Frequency Divider Fabricated in a Commercial SiGe Bipolar Technology," *European Microwave Conference, EuMC 2002*, Sept. 23–27, Milano, Italy.

[5] B. Neurauter, G. Märzinger, T. Lüftner, R. Weigel, M. Scholz, V. Mutlu, and J. Fenk, "GSM 900/DCS 1800 Fractional-N Frequency Synthesizer with Very Fast Settling Time", *IEEE MTT-S International Microwave Symposium*, Phoenix, AZ, vol. 2, pp. 705–708, 2001.

[6] T. Musch, I. Rolfes, and B. Schiek, "A Highly Linear Frequency Ramp Generator Based on a Fractional Divider Phase-Locked-Loop," *IEEE Trans. Instrumentation and Measurement*, vol. 48, no. 2, pp. 634-637, April 1999.

[7] T. Musch and B. Schiek, "Measurement of the ramp linearity of extremely linear frequency ramps using a fractional dual loop structure," *IEEE Trans. Instrumentation and Measurement*, vol. 50, no. 2, pp. 389-392, 2001.

[8] A. D. Poularikas, *The transforms and applications handbook*, 2nd ed. Boca Raton, Fla.: CRC Press, 2000